XIAOLING,YI

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HomePage: https://xiaolingyi.github.io

EDUCATION

KU Leuven Leuven, Belgium
Ph.D. in Engineering Science *Sep 2023 - Present*

- Multi-core machine learning chips

Fudan University Shanghai, China
M.S. in Integrated Circuits and Systems Design *Sep 2020 - Jun 2023*

- GPA: 3.56/4 (Rank: Not available)
- Research interests: Computer Architecture, Design Space Exploration, AI Accelerators Design, AI Accelerators High-level Modeling, Electronic Design Automation (EDA)

Fudan University Shanghai, China
B.E. in Microelectronic Science and Engineering *Sep 2016 - Jun 2020*

- GPA: 3.67/4.0 (Rank: top 10%)
- Relevant coursework: Computer Architecture, Design of Integrated Circuits, Principles and Applications of FPGA, Mathematical Statistics and Stochastic Process, Signal and System, Data Structure and Algorithm Design

University of Alberta Alberta, Canada
Exchange student *Jul 2019 - Aug 2019*

- Focused on learning academic writing and public speaking

PUBLICATIONS

- **Xiaoling Yi**, Jialin Lu, Xiankui Xiong, Dong Xu, Li Shang and Fan Yang, "Graph Representation Learning for Microarchitecture Design Space Exploration," Design Automation Conference (DAC), 2023.
- **Xiaoling Yi**, Jiangnan Yu, Zheng Wu, Xiankui Xiong, Dong Xu, Chixiao Chen, Jun Tao, Fan Yang, "NNASIM: an Efficient Event-Driven Simulator for DNN Accelerators with Accurate Timing and Area Models," IEEE International Symposium on Circuits and Systems (ISCAS), 2022.
- Zheng Wu, Wuzhen Xie, **Xiaoling Yi**, Haotao Yang, Ruiyao Pu, Xiankui Xiong, Haidong Yao, Chixiao Chen, Jun Tao, Fan Yang, "An Automated Compiler for RISC-V Based DNN Accelerator," IEEE International Symposium on Circuits and Systems (ISCAS), 2022.
- Jiangnan Yu, Fan Yang, **Xiaoling Yi**, Chixiao Chen, Jun Tao, Dong Xu, Xiankui Xiong, Haotao Yang,"TNoC: A Flexible Topology Reconfigurable NoC Generator for Manycore DNN Accelerators," Great Lakes Symposium on VLSI, 2023.
- Wu, Zheng, **Xiaoling Yi**, Li Shang, and Fan Yang. "SenseDSE: Sensitivity-Based Performance Evaluation for Design Space Exploration of Microarchitecture." In 2024 Design, Automation Test in Europe Conference Exhibition (DATE), pp. 1-6. IEEE, 2024.
- Wu, Zheng, Jinyi Shen, **Xiaoling Yi**, Li Shang, Fan Yang, and Xuan Zeng. "Prior-Boosted GRL: Microarchitecture Design Space Exploration via Graph Representation Learning." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2024).

RESEARCH EXPERIENCE

Fudan University (State Key Laboratory of Integrated Chips and Systems) Shanghai, China
Research Assistant to Prof. Fan Yang *Jul 2020 - June 2023*

- BOOM (Berkeley Out-of-order Machine) microarchitecture exploration with graph representation learning
- AI accelerator design, FPGA prototype, and high-level modeling

INTERNSHIP

DAMO Academy, Alibaba Group Shanghai, China

Research Intern *Mar 2023 - Aug 2023*

- Memory pooling at data center using CXL
- Special functional unit hardware design and verification

Advanced Micro Devices, Inc Shanghai, China

System Design Intern *Jul 2022 - Sep 2022*

- Performed Intern duties, focused on x86 SoC architecture, firmware basic, and low power design practices

CONTEST EXPERIENCE

- 1st Place Award, CAD Contest at International Conference on Computer-Aided Design (ICCAD) 2022 (top 1) 2022
- National 1st Prize, Integrated Circuit EDA Elite Challenge (top 5 %) 2021
- National 2nd Prize, China Post-Graduate Mathematical Contest in Modeling (top 15 %) 2021
- National 3rd Prize, National College Students Electronic Design Competition (top 20 %) 2019

SELECTED AWARDS AND HONORS

- Outstanding Graduate of Fudan University (top 5 %) 2023
- Excellent Master Thesis of Fudan University (top 5 %) 2023
- College Graduate Excellence Award of Shanghai (top 5 %) 2020
- First Prize Scholarship, Fudan University (top 5 %) 2021, 2019
- Outstanding Student of Fudan University (top 5 %) 2018
- Second Prize Scholarship, Fudan University (top 15 %) 2017, 2018, 2020, 2022

TEACHING

Fudan University Shanghai, China

Teaching Assistant *Sep 2020 - Jun 2021*

- Performed TA duties for Fundamentals of Computer Software, Spring 2021 (instructor: Prof. Changhao Yan)
- Performed TA duties for System-Level FPGA Design, Fall 2020 (instructor: Prof. Lingli Wang and Dr. Xuegong Zhou)